CLAIMS

What is claimed is:

1. A device for transmitting register data to external data terminals of a memory device, the memory device operable to output a first plurality of data bits from a memory array to the external terminals responsive to a first addressing signal, comprising:

a register operable to store a second plurality of data bits and to output the second plurality of bits responsive to a second addressing signal;

a coupling circuit coupled to the register to receive the second plurality of data bits, the coupling circuit operable to output a third plurality of bits corresponding to the second plurality of bits responsive to an enabling signal; and

a data path circuit coupled to the memory array to receive the first plurality of data bits, to the coupling circuit to receive the third plurality of data bits, and to the external terminals, the data path circuit operable to transmit the data bits received to the external terminals of the memory device.

2. The device of claim 1 wherein each of the third plurality of data bits respectively comprises the complement of each of the second plurality of data bits.

3. The device of claim 1 wherein the coupling circuit comprises:

a first plurality of bus driver stages, each of the first plurality of bus driver stages operable to output one of the third plurality of data bits corresponding to a respective one of the second plurality of data bits responsive to the enabling signal; and

a second plurality of bus driver stages, each of the second plurality of bus driver stages operable to output a one of the third plurality of data bits responsive to the enabling signal, each of the data bits output by the second plurality of bus driver stages having a first logic level.

4. The device of claim 3 wherein the first logic level comprises a logic zero.

5. The device of claim 1 wherein each of the first plurality of bus driver stages comprises:

an inverter operable to receive one of the second plurality of data bits and to generate the complement of the data bit in response to receiving the data bit;

a nand gate coupled to the inverter to receive the complement of the data bit and operable to receive the enabling signal, the nand gate operable to produce a first output signal corresponding to the logic states of the complement of the data bit and the enabling signal;

a nor gate coupled to the inverter to receive the complement of the data bit and operable to receive the complement of the enabling signal, the nor gate operable to produce a second output signal corresponding to the logic states of the complement of the data bit and the complement of the enabling signal;

a first transistor having a gate, a source, and a drain, the gate coupled to the nand gate to receive the first output signal, the source coupled to a first voltage source, the first transistor conducting when the first output signal is in a first state; and

a second transistor having a gate, a source, and a drain, the gate coupled to the nor gate to receive the second output signal, the source coupled to a second voltage source, and the drain coupled to the drain of the first transistor, the second transistor conducting when the second output signal is in a second state, and the drain of the second transistor operable to generate one of the second plurality of data bits, each of the third plurality of data bits being output from the respective drain of the second transistor.

6. The device of claim 1 wherein each of the second plurality of bus driver stages comprises:

an inverter operable to be coupled to a third voltage source to receive a third voltage, and to generate the complement of the data bit in response to receiving the third voltage;

a nand gate coupled to the inverter to receive the complement of the third voltage and operable to receive the enabling signal, the nand gate operable to produce a first output signal corresponding to the logic states of the complement of the third voltage and the enabling signal;

a nor gate coupled to the inverter to receive the complement of the third voltage and operable to receive the complement of the enabling signal, the nor gate operable to produce a second output signal corresponding to the logic states of the complement of the third voltage and the complement of the enabling signal;

a first transistor having a gate, a source, and a drain, the gate coupled to the nand gate to receive the first output signal, the source coupled to the first voltage source, the first transistor conducting when the first output signal is in a first state; and

a second transistor having a gate, a source, and a drain, the gate coupled to the nor gate to receive the second output signal, the source coupled to a second voltage source, and the drain coupled to the drain of the first transistor, the second transistor conducting when the second output signal is in a second state, and the drain of the second transistor operable to generate one of the second plurality of data bits, each of the third plurality of data bits being output from the respective drain of the second transistor.

7. The device of claim 1 wherein the second plurality of data bits comprises thirty two data bits.

8. The device of claim 1 wherein the third plurality of data bits comprises sixty four data bits.

9. The device of claim 1 wherein the data path circuit comprises a multiplexer coupled between the coupling circuit and the external terminals, the multiplexer operable to receive the third plurality of data bits and to sequentially output a plurality of portions of the third plurality of data bits responsive to a control signal, and operable to receive the first plurality of data bits from the memory device and to sequentially output a plurality of portions of the first plurality of data bits responsive to the control signal, the multiplexer operable to receive only one of the first and third pluralities of data bits at any given time.

10. A device for transmitting register data to data terminals of a memory device, comprising:

a column address bus operable to couple a register address signal;

a decoder coupled to the column address bus to receive the register address signal and operable to produce a register address responsive to the register address signal;

a register coupled to the decoder to receive the register address and operable to output a first plurality of data bits stored in the register corresponding to the register address;

a register driver circuit coupled to the register to receive the first plurality of data bits, the register driver circuit operable to generate a respective second plurality of data bits corresponding to the first plurality of data bits responsive to a selector signal;

a first set of interim storage latches coupled to the register driver circuit to receive a first portion of the second plurality of data bits, each interim storage latch in the first set operable to latch data from the register driver circuit responsive to a first activation signal;

a second set of interim storage latches coupled to the register driver circuit to receive a second portion of the second plurality of data bits, each interim storage latch in the second set operable to latch data from the register driver circuit responsive to a second activation signal;

a multiplexing circuit coupled to respective first latches to receive the first portion of the second plurality of data bits and to respective second latches to receive the second portion of the second plurality of data bits, the multiplexing circuit operable to sequentially transmit the first portion of the second plurality of data bits responsive to a control signal having a first state and the second portion of the second plurality of data bits responsive to the control signal having a second state;

a timing control circuit operable to receive a first clock signal and to generate the first and second activation signals responsive to the first clock signal and to respectively apply the first and second activation signals to the first and second sets of latches, the timing control circuit further being responsive to the first clock signal to provide the control signal having the first state to the multiplexing circuit during a first portion of a selected clock cycle and to provide the control signal having the second state to the multiplexing circuit during a second portion of the selected clock cycle;

an output data buffer coupled to the multiplexing circuit to sequentially receive the first and second portions of the second plurality of data bits, the output data buffer operable to sequentially transmit the first and second portions responsive to a second clock signal;

a driver circuit coupled to the data terminals of the memory device, and to the output data buffer to receive the first and second portions of the second plurality of data bits, the driver circuit operable to sequentially transmit the first and second portions of the second plurality of data bits to the data terminals.

11. The device of claim 10 wherein the driver circuit generates and transmits a data clock signal to at least one of the data terminals in synchronization with the transmission of the first and second portions of the second plurality of data bits.

12. The device of claim 10 wherein:

the output data buffer generates a third and fourth clock signals; and

the driver circuit is coupled to the output data buffer to receive the third and fourth clock signals, and is operable to transmit the first and second portions of the second plurality of data bits responsive to the third and fourth clock signals.

13. The device of claim 12 wherein the fourth clock signal comprises a quadrature clock with respect to the third clock signal.

14. The device of claim 10 wherein the first address signal comprises a register address, and further comprising:

an address selector circuit coupled between the decoder and the column address bus, the address selector circuit operable to receive a column address signal, the register address signal, and the selector signal, and operable to output the column address to the column address bus when the selector signal is in a first state, and to output the register address signal to the column address bus when the selector signal is in a second state.

15. The device of claim 14, further comprising:

a pass gate operable to receive the selector signal and a command signal, and to transmit the command signal to an output node responsive to the selector signal being in a first state, the command signal operable to cause the memory device to enter a condition that prevents data from being written to the memory device when the command signal is in a first state; and

a write disabling circuit coupled to the output node of the pass gate, the write disabling circuit operable to receive the selector signal and to bias the command signal to the first state responsive to the selector signal being in a second state.

16. The device of claim 15 wherein the first state of the command signal comprises a logic zero, and the write disabling circuit couples the output node of the pass gate to ground responsive to the selector signal being in the second state.

17. The device of claim 15 wherein the write disabling circuit comprises a transistor coupled between the output node of the pass gate circuit and ground, the transistor operable to couple the output node to ground responsive to the selector signal being in the second state.

18. The device of claim 14 wherein the first state of the selector signal comprises a logic zero and the second state of the selector signal comprises a logic one.

19. The device of claim 14 wherein the address selector circuit comprises:

an inverter operable to receive the selector signal and to generate the complement of the selector signal in response to receiving the selector signal;

a first pass gate operable to receive the column address signal, the complement of the selector signal from the inverter, and the selector signal, and operable to couple the column address signal to the column address bus responsive to the selector signal having the first state; and

a second pass gate operable to receive the register address signal, the complement of the selector signal from the inverter, and the selector signal, and operable to couple the register address signal to the column address bus responsive to the selector signal having the second state.

20. The device of claim 10 wherein the register driver circuit comprises a plurality of register driver stages, one stage per each data bit of the first plurality of data bits, each register driver stage comprising:

an inverter operable to receive one of the second plurality of data bits and to generate the complement of the data bit in response to receiving the data bit;

a nand gate coupled to the inverter to receive the complement of the data bit and operable to receive the selector signal, the nand gate operable to produce a first

output signal corresponding to the logic states of the complement of the data bit and the selector signal;

a nor gate coupled to the inverter to receive the complement of the data bit and operable to receive the complement of the selector signal, the nor gate operable to produce a second output signal corresponding to the logic states of the complement of the data bit and the complement of the selector signal;

a first transistor having a gate, a source, and a drain, the gate coupled to the nand gate to receive the first output signal, the source coupled to a first voltage source, the first transistor conducting when the first output signal is in a first state; and

a second transistor having a gate, a source, and a drain, the gate coupled to the nor gate to receive the second output signal, the source coupled to a second voltage source, and the drain coupled to the drain of the first transistor, the second transistor conducting when the second output signal is in a second state, and the drain of the second transistor operable to generate one of the second plurality of data bits.

21. The device of claim 20 wherein:

the first output signal is in the first state when the first output signal comprises a logic zero and is in a second state when the first output signal comprises a logic one; and

the second output signal is in a first state when the second output signal comprises a logic zero and is in the second state when the second output signal comprises a logic one.

22. The device of claim 20 wherein the first voltage source comprises a relatively high voltage, and the second voltage source comprises a relatively low voltage.

23. The device of claim 22 wherein the first voltage source comprises V_{cc} and the second voltage source comprises ground.

24. The device of claim 20 wherein the register driver circuit further comprises a second plurality of register stages, each stage operable to produce a third plurality of data bits when the selector signal is in the second state;

the first set of interim storage latches are further coupled to the register driver circuit to receive a first portion of the third plurality of data bits;

the second set of interim storage latches are further coupled to the register driver circuit to receive a second portion of the third plurality of data bits;

the multiplexing circuit is further coupled to respective first latches to receive the first portion of the second and third pluralities of data bits and to respective second latches to receive the second portion of the second and third pluralities of data bits, the multiplexing circuit operable to sequentially transmit the first portion of the second and third pluralities of data bits responsive to the first control signal and the second portion of the second and third pluralities of data bits responsive to the second control signal;

the output data buffer is further coupled to the multiplexing circuit to sequentially receive the first and second portions of the second and third pluralities of data bits, and is operable to sequentially transmit the first and second portions responsive to the second clock signal; and

the driver circuit is further coupled to the output data buffer to receive the first and second portions of the second and third pluralities of data bits, the driver circuit being operable to sequentially transmit the first and second portions of the second and third pluralities of data bits to the data terminals.

25. The device of claim 24 wherein the each of the third plurality of data bits comprise a first logic level.

26. The device of claim 25 wherein the first logic level comprises a logic zero.

27. The device of claim 24 wherein the register driver circuit comprises a plurality of register driver stages, one stage per each data bit of the first plurality of data bits, each register driver stage comprising:

an inverter operable to be coupled to a third voltage source to receive a third voltage, and to generate the complement of the data bit in response to receiving the third voltage;

a nand gate coupled to the inverter to receive the complement of the third voltage and operable to receive the selector signal, the nand gate operable to produce a first output signal corresponding to the logic states of the complement of the third voltage and the selector signal;

a nor gate coupled to the inverter to receive the complement of the third voltage and operable to receive the complement of the selector signal, the nor gate operable to produce a second output signal corresponding to the logic states of the complement of the third voltage and the complement of the selector signal;

a first transistor having a gate, a source, and a drain, the gate coupled to the nand gate to receive the first output signal, the source coupled to the first voltage source, the first transistor conducting when the first output signal is in a first state; and

a second transistor having a gate, a source, and a drain, the gate coupled to the nor gate to receive the second output signal, the source coupled to a second voltage source, and the drain coupled to the drain of the first transistor, the second transistor conducting when the second output signal is in a second state, and the drain of the second transistor operable to generate one of the second plurality of data bits.

28. The device of claim 27 wherein the third voltage source comprises a voltage equivalent to a logic one.

29. The device of claim 10 wherein each of the respective second plurality of data bits corresponds to the complement of the first plurality of data bits.

30. The device of claim 10 wherein the first and second portions of the second plurality of data bits comprise the second plurality of data bits.

31. The device of claim 10 wherein the memory device has a sense-amplifier circuit, and the register driver circuit is further coupled between the sense-amplifier circuit and the first and second sets of interim storage latches, the sense-amplifier circuit being disabled when the selector signal is in the second state.

32. The device of claim 30 wherein the sense-amplifier circuit is tri-stated when disabled.

33. A packetized dynamic random access memory, comprising:

at least one array of memory cells operable to store a first plurality of data bits at respective locations determined by a row address and a column address;

a row address circuit coupled to each array, the row address circuit operable to receive and decode the row address, and to select a row of memory cells corresponding to the row address responsive to a first set of command signals;

a column address circuit coupled to each array, the column address circuit operable to receive data bits from or apply data bits to one of the memory cells in the selected row corresponding to the column address responsive to a second set of command signals;

a command buffer operable to receive command packets and initialization packets, and to generate respective command words and initialization words corresponding to each received command packet and initialization packet, respectively;

a register operable to store a second plurality of data bits and to output the second plurality of bits responsive to an addressing signal;

a coupling circuit coupled to the register to receive either data bits from the memory cells of the array responsive to the second set of command signals or the second plurality of data bits from the register, the coupling circuit operable to output a

third plurality of bits corresponding to the received data bits responsive to an enabling signal; and

a data path circuit operable to couple the third plurality of bits from the coupling circuit to a data bus responsive to a third set of command signals.

34. The packetized dynamic random access memory of claim 33 wherein the coupling circuit comprises:

a first plurality of bus driver stages, each of the first plurality of bus driver stages operable to output one of the third plurality of data bits corresponding to a respective one of the second plurality of data bits responsive to the enabling signal; and

a second plurality of bus driver stages, each of the second plurality of bus driver stages operable to output a one of the third plurality of data bits responsive to the enabling signal, each of the data bits output by the second plurality of bus driver stages having a first logic level.

35. The packetized dynamic random access memory of claim 34 wherein the first logic level comprises a logic zero.

36. The packetized dynamic random access memory of claim 33, further comprising a multiplexer coupled between the coupling circuit and the data bus, the multiplexer operable to receive the third plurality of data bits and to sequentially output to the data bus a plurality of portions of the third plurality of data bits responsive to a control signal, and operable to receive the first plurality of data bits from the memory device and to output to the data bus a plurality of portions of the first plurality of data bits responsive to the control signal, the multiplexer operable to receive only one of the first and third pluralities of data bits at any given time.

37. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a packetized dynamic random access memory coupled to the processor bus, comprising,

at least one array of memory cells operable to store a first plurality of data bits at respective locations determined by a row address and a column address;

a row address circuit coupled to each array, the row address circuit operable to receive and decode the row address, and to select a row of memory cells corresponding to the row address responsive to a first set of command signals;

a column address circuit coupled to each array, the column address circuit operable to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to a second set of command signals;

a command buffer operable to receive command packets and initialization packets, and to generate respective command words and initialization words corresponding to each received command packet and initialization packet, respectively;

a register operable to store a second plurality of data bits and to output the second plurality of bits responsive to an addressing signal;

a coupling circuit coupled to the register to receive either data bits from the memory cells of the array responsive to the second set of command signals or the second plurality of data bits from the register, the coupling circuit operable to output a third plurality of bits corresponding to the received data bits responsive to an enabling signal; and

a data path circuit operable to couple the third plurality of bits from the coupling circuit to a data bus responsive to a third set of command signals

38. The computer system of claim 37 wherein the coupling circuit comprises:

a first plurality of bus driver stages, each of the first plurality of bus driver stages operable to output one of the third plurality of data bits corresponding to a respective one of the second plurality of data bits responsive to the enabling signal; and

a second plurality of bus driver stages, each of the second plurality of bus driver stages operable to output a one of the third plurality of data bits responsive to the enabling signal, each of the data bits output by the second plurality of bus driver stages having a first logic level.

39. The computer system of claim 38 wherein the first logic level comprises a logic zero.

40. The computer system of claim 37, further comprising a multiplexer coupled between the coupling circuit and the data bus, the multiplexer operable to receive the third plurality of data bits and to sequentially output to the data bus a plurality of portions of the third plurality of data bits responsive to a control signal, and operable to receive the first plurality of data bits from the memory device and to output to the data bus a plurality of portions of the first plurality of data bits responsive to the control signal, the multiplexer operable to receive only one of the first and third pluralities of data bits at any given time.

41. A method for reading register data of a memory device, the memory device operable to transmit data from a memory array in a predetermined format to an external terminal via an output data path, comprising:

reading the contents of a register;

converting the contents of the register to the predetermined format;

decoupling the output data path from the memory array; and

applying the contents of the register in the predetermined format to the external terminal via the output data path.

42. The method of claim 41 wherein the predetermined format comprises a plurality of data bits in parallel.

43. The method of claim 42 wherein the plurality of data bits comprises sixteen data bits.

44. The method of claim 41 wherein converting the contents of the register to the predetermined format comprises:

dividing the contents of the register into portions; and

multiplexing the portions of the contents of the register.

45. The method of claim 44 wherein dividing the contents of the register into portions comprises dividing the contents of the register into equal portions.

46. A method for addressing a register of a memory device having a memory array operable to receive a memory address via an address bus, the method comprising:

coupling the register to the address bus; and

applying a register address to the address bus.

47. The method of claim 46 wherein the register address is coupled to the address bus when the register is addressed, and otherwise is not coupled to the address bus.

48. The method of claim 46 wherein the address bus comprises a column address bus and the memory address comprises a column address.

49. The method of claim 46, further comprising:

decoding the address applied to the address bus; and

wherein applying the address to the register comprises applying the address to the register when the coded address has predetermined characteristics.